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10/040,608	12/28/2001	Doron Orenstien	P10720	2677

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	2

DATE MAILED: 12/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/040,608	Applicant(s) ORENSTIEN ET AL.	
	Examiner Tuan V. Thai	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Part III DETAILED ACTION

Specification

1. Claims 1-30 are presented for examination.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Claim Objections - 35 CFR 1.75

3. Claim 4 is objected to under 37 CFR 1.75(b) as not substantially differing from claim 3.

The claim as written do not appear to be substantially different or to provide substantially different patent protection.

Applicants are required to 1) cancel the objected to claims, (2) amend the claims so that they are substantially different from any other claims, or (3) provide sufficient reasons why the claims as presently written are substantially different or provide substantially different patent protection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-30 are rejected under 35 U.S.C. § 102(b) as being anticipated by Hewitt et al. (USPN: 6,085,330); hereinafter Hewitt.

As per claims 1, 13, 21 and 27; Hewitt discloses the invention as claimed including method for accessing a cache and a computer system comprising processor 102 comprising an L1 cache 104 with a first and second bus interface (e.g. see figure 1); a high power bus 110 (e.g. see figure 1), a low power bus 114 (e.g. see figure 1); a high power bus interface coupled to the high power bus 110 is taught as north bridge 108 coupled to high power bus 110, and south bridge 116 as the low power bus interface coupled to the low power bus 114 (e.g. see figure 1; column 3, lines 43 et seq.); it should be further noted that the lower power bus 114 (PCI bus) is known be narrower than the system bus 110 wherein Hewitt further discloses low power interface coupled to the low power bus 114 having clock line as clock signal STPCLK# connected directly to the processor 102 for generating a stop processor signal STPCPU# on a line that is connected to the system PLL 120 (e.g. see column 3, lines 55 et seq.); the further limitation of a controller (system PLL 120, north bridge 108, and

south bridge 116) to communicate with the processor 102 via the high power bus during a high power mode of operation and to communicate with the processor 102 via the low power bus during a low power mode of operation is taught by Hewitt to the extent that it is being claimed; for example, Hewitt clearly discloses the L1 cache memory 104 can be accessed via various buses (e.g. see column 2, lines 5-6), typically host/high-power bus 110 and PCI/low-power bus 114; wherein the cache is normally snooped during fully-operational C0 thru host bus 110; when in C2 state which is a low state but also a state in which the PCI cycle is allowed to snoop the internal cache 104 via PCI bus 114 (normal protocol) (e.g. see column 4, lines 35 et seq.);

As per claim 2, Hewitt discloses the first bus as being equivalent to the host/high power bus 110 coupled to the north bridge 108, and the second bus as the PCI bus 114 coupled to the south bridge 116 (e.g. see figure 1); it is further known and inherent in the art that the secondary bus 114 is commonly implemented to be smaller than the primary bus or host bus 110;

As per claims 3 and 4, Hewitt discloses system memory 112, peripheral devices (bus master, various devices; column 2, line 5); the peripheral device to request an access of the main memory via the controller (e.g. see column 2, lines 7 et seq.);

As per claim 5, Hewitt discloses the first mode (C0) of operation is a high power mode (fully operational state); and the

second mode of operation (C2) is a low power mode wherein CPU cache can still be snooped (e.g. see column 1, lines 36 et seq.);

As per claim 6, Hewitt discloses during the low power mode of operation, the stop clock signal STPCLK# is generated by South Bridge 116 connected directly to the CPU 102 for generating a stop processor signal STPCPU# on a line that is connected to the system PLL 120 wherein CPU 102 and northbridge 108 are powered down (e.g. see column 3, lines 55 et seq.);

As per claims 7 and 8, Hewitt discloses the clock generator for providing the first clock signal/second clock signal for timing operation of the processor (e.g. see column 7, lines 38 et seq.; column 8, lines 23 et seq.); STPCLK# clock signal and STPCPU# signal for first and second mode of operation (e.g. see column 5, lines 37 et seq.);

As per claim 9, the further limitation of the phase-locked-loop within processor, and the second clock signal is routed through the phase-lock-loop before being provided to the cache during the low-power mode of operation (e.g. see column 3, lines 32 et seq.; column 6, lines 1 et seq.);

As per claim 10; see argument with respect to claim 2; in addition, it is inherent that high power bus consumes more power during the high power mode of operation than during the low power mode of operation;

As per claim 11, Hewitt discloses the north bridge 108 and

south bridge 116 coupled to the system PLL 120 thru the second bus as the PCI 114 (e.g. see figure 1); wherein it is inherent that the PCI bus 114 having clock line, data line and control line;

As per claim 12; Hewitt further discloses the north bridge 108 and south bridge 116 coupled to the system PLL 120 thru the host bus 110; wherein it can be see from figure 1 that the host bus is implemented as parallel bus connected to multiple devices including L2 external cache 106 and CPU 102 and other devices (e.g. see also column 3, lines 39 et seq.); wherein the PCI bus 114 is a single line data bus connected to the south bridge 116 and ISA bus 118 (e.g. see figure 1);

As per claim 14, Hewitt discloses system memory 112, peripheral devices (bus master, various devices; column 2, line 5); the peripheral device to request an access of the main memory via the controller (e.g. see column 2, lines 7 et seq.);

As per claim 15, Hewitt discloses the first mode (C0) of operation is a high power mode (fully operational state); and the second mode of operation (C2) is a low power mode wherein CPU cache can still be snooped (e.g. see column 1, lines 36 et seq.); wherein during the low power mode operation (C2), the signaling circuit allows a grant of the PCI Bus 114 by the north bridge 108 (idling of the high power bus 110) to enter low power mode operation (e.g. see column 5, lines 61 et seq.);

As per claim 16, Hewitt discloses the first mode (C0) of operation is a high power mode (fully operational state) in which the local cache can be snooped for change in data update; and the second mode of operation (C2) is a low power mode wherein CPU cache can still be snooped (e.g. see column 1, lines 36 et seq.);

As per claims 17 and 18; Hewitt discloses the clock generator for providing the first clock signal/second clock signal for timing operation of the processor (e.g. see column 7, lines 38 et seq.; column 8, lines 23 et seq.); STPCLK# clock signal and STPCPU# signal for first and second mode of operation (e.g. see column 5, lines 37 et seq.);

As per claim 19; the further limitation of a power supply to provide a lower voltage supply to the processor during the low power mode of operation than during the high power mode of operation is taught by Hewitt since Hewitt clearly discloses that the power consumption during the (C2) state (low power state) is about 10% of the high power (C0) state (e.g. see column 1, lines 50 et seq.);

As per claim 20; Hewitt further discloses the north bridge 108 and south bridge 116 coupled to the system PLL 120 thru the host bus 110; wherein it can be see from figure 1 that the host bus is implemented as parallel bus connected to multiple devices including L2 external cache 106 and CPU 102 and other devices (e.g. see also column 3, lines 39 et seq.); wherein the PCI bus

114 is a single line data bus connected to the south bridge 116 and ISA bus 118 (e.g. see figure 1);

As per claim 22, Hewitt discloses during the low power mode of operation, the stop clock signal STPCLK# is generated by South Bridge 116 connected directly to the CPU 102 for generating a stop processor signal STPCPU# on a line that is connected to the system PLL 120 wherein CPU 102 and northbridge 108 are powered down (e.g. see column 3, lines 55 et seq.);

As per claim 23, Hewitt further discloses the first bus as being equivalent to the host/high power bus 110 coupled to the north bridge 108, and the second bus as the PCI bus 114 coupled to the south bridge 116 (e.g. see figure 1); in addition, it is known and inherent in the art that the secondary bus 114 is commonly implemented to be smaller than the primary bus or host bus 110;

As per claim 24, Hewitt discloses the low power bus 114 coupled to the south bridge 116, ISA bus 118 and system PLL 120, which provides higher supports for source-synchronizations operation than that of the host/high-power bus 110 (e.g. see figure 1);

As per claim 25, Hewitt discloses the first and second phase-locked-loop within processor to provide the clock signals to the cache memory regions during the high and low power mode (e.g. see column 3, lines 32 et seq.; column 6, lines 1 et seq.);

As per claim 26, a memory bus interface is taught and embedded within the system of Hewitt (e.g. see figure 1);

As per claim 28, Hewitt discloses that to enter the low power mode, (C2) state, the PCI REQ# request signal is asserted; at the same time the high power bus 110 is known to be powered down (e.g. column 3, line 55 bridging column 4, line 41);

As per claim 29, the further limitation of snooping the cache via the low power bus including providing a clock signal to the cache via the low power bus is being equivalent to the process of de-asserting the STPCPU# signal to allow snooping of the internal cache 104 when in the low power mode (e.g. see column 4, lines 31 et seq.);

As per claim 30, Hewitt discloses that in response to the signal for entering the low power mode, the processor 102 flushes instructions which known to be in the cache 104, completes all pendings and in-progress bus cycles, stops the processor internal clock and enters the stop clock state if system logic stops the bus clock CLK (e.g. see column 3, line 64 bridging column 4, line 1);

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is 703-305-3842.

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The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM. The examiner can also be reached on alternate Fridays or e-mailed at ***tuan.thai@uspto.gov;***

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Matthew M. Kim can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900. The Official Fax Numbers for TC-2100 is ***(703) 872-9306***

TVT/December 14, 2003

Tuan V. Thai
PRIMARY EXAMINER
Group 2100